List of Claims:

1. (Currently Amended) A phase-locked loop (PLL) system having active times and inactive times, the system comprising:

an apparatus configured to provide charge;

a voltage-controlled oscillator (VCO) having a VCO input coupled and configured to receive charge from the apparatus, a tuning voltage at the VCO input being at a VCO-lock voltage when the phase-locked loop system is locked to a frequency; and

a controller coupled to the apparatus and configured to provide a control signal to the apparatus to control the charge provided by the apparatus;

wherein the apparatus is configured to provide, during at least a portion of an inactive time of the PLL system and in response to the control signal, charge such that the tuning voltage at the VCO input is approximately at the VCO-lock voltage at ~~the~~ a start of an active time of the PLL system; and

wherein during the inactive time of the PLL at least one component of the PLL for locking to a frequency is inoperative.

2. (Original) The system of claim 1 wherein the apparatus includes a current supply that is configured to supply the charge during at least a portion of an inactive time of the system.

3. (Original) The system of claim 2 wherein the current supply is configured to provide a compensating current during substantially an entire inactive time between active times.

4. (Currently Amended) The system of claim 2 wherein the current supply includes a plurality of current sub-supplies configured to provide discrete current amounts that are related to each other in a binary progression.

5. (Original) The system of claim 2 wherein the current supply includes a plurality of current mirrors.

6. (Original) The system of claim 5 wherein the plurality of current mirrors are

coupled to selectively provide current from multiple current supplies to a common destination concurrently.

7. (Original) The system of claim 1 wherein the apparatus includes a charge pump configured to provide the sufficient energy during an initial portion of the inactive time.

8. (Original) The system of claim 7 wherein the initial portion constitutes less than about 0.001% of the inactive time.

9. (Original) The system of claim 1 wherein the active time of the PLL system is an initial active time of the PLL system.

10. (Currently Amended) The system of claim ~~9~~ 1 wherein the controller is configured to retrieve information from a memory to provide the control signal.

11. (Original) The system of claim 1 wherein the controller is coupled to the VCO and is configured to receive an indication of a beginning tuning voltage at the VCO input at the start of an active time of the PLL system and an indication of the VCO-lock voltage, and to determine the control signal using the indications of the beginning tuning voltage and the VCO-lock voltage.

12. (Original) The system of claim 11 wherein the controller is configured to determine the control signal based upon a difference between the VCO-lock voltage and a voltage related to the beginning tuning voltage.

13. (Original) The system of claim 12 wherein the active time of the PLL system is at least a second active time of the PLL system following at least a first, previous, active time of the PLL system.

14. (Original) The system of claim 12 wherein the related voltage is the beginning voltage.

15. (Original) The system of claim 12 further comprising a filter coupled to receive signals with corresponding charge from the apparatus, to filter the signals received from the apparatus, and to provide output signals with associated charge to the VCO in response to the received signals.

16. (Original) The system of claim 1 wherein the active time of the PLL system is at least a second active time of the PLL system following at least a first, previous, active time of the PLL system, where the VCO-lock voltage is a first VCO-lock voltage when the phase-locked loop system is locked to a first frequency during the first active time of the PLL system, the tuning voltage at the VCO input being at a second VCO-lock voltage when the phase-locked loop system is locked to a second frequency, and where the apparatus is configured to provide, during at least a portion of an inactive time of the PLL system and in response to the control signal, charge such that the tuning voltage at the VCO input is approximately at the second VCO-lock voltage at the start of the second active time of the PLL system.

17. (Original) A method comprising:

activating a phase-locked loop (PLL), including a voltage-controlled oscillator (VCO), to lock onto a frequency, a tuning voltage of the VCO being at a VCO-lock voltage when the PLL is locked;

determining a difference between the tuning voltage approximately at an activation time of the PLL and the VCO-lock voltage;

deactivating the PLL; and

providing charge, in an amount depending upon the difference, to the VCO during at least a portion of a deactivation time when the PLL is deactivated to affect the tuning voltage of the VCO.

18. (Original) The method of claim 17 further comprising reactivating the PLL when

the tuning voltage is approximately equal to the VCO-lock voltage.

19. (Original) The method of claim 17 wherein the VCO-lock voltage is a first VCO-lock voltage corresponding to the PLL being locked to a first frequency, the method further comprising reactivating the PLL when the tuning voltage is approximately equal to a second VCO-lock voltage corresponding to the VCO tuning voltage for the PLL to be locked to a second frequency that is different from the first frequency.

20. (Original) The method of claim 17 wherein the providing provides sufficient charge to compensate for charge leakage during deactivation of the PLL.

21. (Currently Amended) The method of claim 17 wherein the providing includes substantially continuously providing at least one amount of current from among a plurality of discrete amounts of current.

22. (Currently Amended) The method of claim 21 wherein the plurality of discrete amounts of current are related to each other by a binary progression.

23. (Original) The method of claim 21 further comprising selecting at least one of a plurality of current mirrors to provide the at least one amount of current.

24. (Original) The method of claim 17 wherein the providing includes supplying charge from a charge pump for at least an initial portion of the deactivation time.

25. (Original) The method of claim 24 wherein the portion is dependent upon the indication.

26. (Original) The method of claim 17 wherein determining the indication includes determining a first indication that is related to the tuning voltage approximately at an activation time of the PLL, and determining the VCO-lock voltage.

27. (Original) The method of claim 26 wherein determining the first indication is performed before a charge pump of the PLL is turned on when activating the PLL.

28. (Original) The method of claim 17 wherein determining the indication includes integrating indicia of activity of a charge pump of the PLL between activating and deactivating the PLL.

29. (Original) The method of claim 28 wherein the integrating includes integrating a number of times the charge pump goes up and down.

30. (Original) The method of claim 29 wherein the integrating includes integrating quantities and polarizations of charge provided by the charge pump.

31. (Original) The method of claim 28 wherein the integrating is performed digitally.

32. (Original) The method of claim 17 wherein determining the indication includes integrating an error signal produced by a phase detector of the PLL.

33. (Original) The method of claim 32 wherein the error signal is transmitted by the phase detector to a charge pump of the PLL.

34. (Original) The method of claim 32 further comprising determining polarity and magnitude of the integration and adjusting the charge provided to the VCO depending on the determined polarity and magnitude.

35. (Original) A phase-locked loop (PLL) comprising:

a voltage-controlled oscillator (VCO) having a VCO input, a tuning voltage at the VCO input being at a VCO-lock voltage when the PLL is locked to a frequency;

means for determining an indication of a difference between the tuning voltage

approximately at an activation time of the PLL and the VCO-lock voltage; and

means for providing charge, in an amount depending upon the indication, to the VCO during at least a portion of a deactivation time when the PLL is deactivated to affect the tuning voltage of the VCO.

36. (Original) The PLL of claim 35 wherein the means for determining compares indicia of the VCO-lock voltage and the tuning voltage at a time near but before the activation time of the PLL.

37. (Original) The PLL of claim 36 wherein the indicia are the VCO-lock voltage and the tuning voltage.

38. (Original) The PLL of claim 35 wherein the means for determining determines amounts and polarities of charge provided to the VCO during at least a portion of the active time of the PLL.

39. (Original) The PLL of claim 38 wherein the at least a portion of the active time is substantially the entire active time.

40. (Original) The PLL of claim 38 wherein the at least a portion of the activate time is a time from the activation time until the PLL is locked.

41. (Original) The PLL of claim 35 wherein the means for determining integrates charge from the means for providing.

42. (Original) The PLL of claim 35 wherein the means for determining integrates an error signal from a phase detector of the PLL.

43. (Original) The PLL of claim 35 wherein the means for providing includes at least one current source.

44. (Currently Amended) The PLL of claim 43 wherein the at least one current source includes a plurality of current sources configured to provide discrete current amounts related to each other in a binary progression.

45. (Currently Amended) A portable telephone comprising:

a battery;

an antenna; and

a receiver coupled to the antenna and to the battery and including a phase-locked loop (PLL) configured to operate in an active mode and a paging mode, the paging mode intermittently activating the PLL to check as to whether an incoming call is being received, the PLL including:

a charge supply;

a voltage-controlled oscillator (VCO) having a VCO input coupled and configured to receive charge from the charge supply, a tuning voltage at the VCO input being at a VCO-lock voltage when the phase-locked loop system is locked to a frequency; and

a controller configured to determine a total amount of charge to provide to the VCO input during a deactivated time period of the PLL to cause the tuning voltage to be approximately equal to the VCO-lock voltage at a beginning of an active time period of the PLL, the controller being further configured to cause the charge supply to provide the total amount of charge to the VCO during at least a portion of the deactivated time period of the PLL;

wherein during the deactivated time period of the PLL at least one component of the PLL for locking to a frequency is inoperative.

46. (Original) The telephone of claim 45 wherein the controller is configured to compare indicia of the tuning voltage approximately at an activation time of the PLL and the VCO-lock voltage.

47. (Original) The telephone of claim 46 wherein the indicia are the tuning voltage and the VCO-lock voltage.

48. (Original) The telephone of claim 45 wherein the charge supply includes at least one current supply.

49. (Currently Amended) The telephone of claim 48 wherein the at least one current supply includes a plurality of current supplies configured to provide discrete current amounts related to each other in a binary progression.

50. (Original) The telephone of claim 46 wherein the controller is configured to determine amounts and polarities of charge provided to the VCO during at least a portion of the active time of the PLL.

51. (Original) The telephone of claim 50 wherein the at least a portion of the active time is substantially the entire active time.

52. (Original) The telephone of claim 51 wherein the at least a portion of the activate time is a time from the activation time until the PLL is locked.

53. (Original) The telephone of claim 45 wherein the controller is configured to integrate charge from the charge supply.

54. (Original) The telephone of claim 45 wherein the controller is configured to integrate an error signal from a phase detector of the PLL.

55. (Original) The telephone of claim 45 wherein the controller is configured to cause the charge supply to provide the total amount of charge to the VCO input during the deactivated time period of the PLL to cause the tuning voltage to change from a deactivated time steady state to approximately the VCO-lock voltage substantially before an active time of the PLL.

56. (Original) The telephone of claim 45 wherein the controller is configured to cause the charge supply to provide the total amount of charge to the VCO during at least a portion of the deactivated time period of the PLL between intermittent active times of the PLL.

57. (Currently Amended) A method comprising:

activating at least a charge pump of a phase-locked loop (PLL) system;

receiving indicia of initial charge to provide by the charge pump to cause a tuning voltage of a voltage-controlled oscillator (VCO) to become at least approximately equal to a VCO-lock voltage from a deactivation steady state of the PLL system, the tuning voltage of the VCO being at the VCO-lock voltage when the PLL system is locked to a frequency;

causing the charge pump to provide the initial charge while at least one component of the PLL system for locking to a frequency is inoperative; and

activating the PLL system when the VCO tuning voltage is approximately equal to the VCO-lock voltage such that the PLL system attempts to lock to a frequency.

58. (Original) The method of claim 57 wherein the receiving includes retrieving the indicia from memory.

59. (Original) The method of claim 57 wherein the activating of at least the charge pump activates less than all portions of the PLL system necessary to allow the PLL system to lock to a frequency.

60. (Original) The method of claim 57 wherein the VCO tuning voltage is approximately zero volts when the VCO is in the deactivation steady state.

61. (Original) The method of claim 57 wherein a capacitor of a resonant circuit of the VCO is substantially completely depleted of charge when the VCO is in the deactivation steady state.

62. (New) The system of claim 4 wherein a smallest of the discrete current amounts is less than an amount that would swing an output of the VCO from one extreme of a desired frequency tolerance of the PLL system to another extreme of the desired frequency tolerance.

63. (New) The method of claim 22 wherein a smallest of the discrete amounts of current is less than an amount that would swing an output of the VCO from one extreme of a desired frequency tolerance of the PLL to another extreme of the desired frequency tolerance.

64. (New) The PLL of claim 44 wherein a smallest of the discrete current amounts is less than an amount that would swing an output of the VCO from one extreme of a desired frequency tolerance of the PLL to another extreme of the desired frequency tolerance.